R-Format:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Op code [31:26] | rs [25:21] | rt [20:16] | Shamt [15:11] | Func [10:5] | Don’t cares |
| 6 | 5 | 5 | 5 | 6 | 5 |

|  |  |  |
| --- | --- | --- |
| Op-code | Func | Instruction |
| 000000 | 000000 | add |
| 000000 | 000001 | comp |
| 000001 | 000000 | and |
| 000001 | 000001 | xor |
| 000010 | 000000 | shll |
| 000010 | 000001 | shrl |
| 000010 | 000010 | shllv |
| 000010 | 000011 | shrlv |
| 000010 | 000100 | shra |
| 000010 | 000101 | shrav |

I-Format:

|  |  |  |  |
| --- | --- | --- | --- |
| Op code [31:26] | rs [25:21] | rt [20:16] | Address/immediate [15:0] |
| 6 | 5 | 5 | 16 |

|  |  |
| --- | --- |
| Op-code | Instruction |
| 010000 | Addi |
| 010001 | compi |
| 010010 | lw |
| 010011 | sw |

J-Format:

|  |  |  |  |
| --- | --- | --- | --- |
| Op code [31:26] | rs [25:21] | Don’t cares | Address [15:0] |
| 6 | 5 | 5 | 16 |

|  |  |
| --- | --- |
| Op-code | Instruction |
| 100000 | b |
| 100001 | br |
| 100010 | bltz |
| 100011 | bz |
| 100100 | bnz |
| 100101 | bl |
| 100110 | bcy |
| 100111 | bncy |

CONTROL SIGNALS:

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Op | Op-code | Func | MemToReg | ALUOp | ALUSrc | RegDst | RegWrite | MemRead | MemWrite | PCSrc |
| add | 000000 | 000000 | 10 | 0001 | 00 | 0 | 1 | 0 | 0 | 00 |
| comp | 000000 | 000001 | 10 | 0010 | 00 | 0 | 1 | 0 | 0 | 00 |
| and | 000001 | 000000 | 10 | 0011 | 00 | 0 | 1 | 0 | 0 | 00 |
| xor | 000001 | 000001 | 10 | 0100 | 00 | 0 | 1 | 0 | 0 | 00 |
| shll | 000010 | 000000 | 10 | 0101 | 01 | 0 | 1 | 0 | 0 | 00 |
| shrl | 000010 | 000001 | 10 | 0110 | 01 | 0 | 1 | 0 | 0 | 00 |
| shllv | 000010 | 000010 | 10 | 0101 | 00 | 0 | 1 | 0 | 0 | 00 |
| shrlv | 000010 | 000011 | 10 | 0110 | 00 | 0 | 1 | 0 | 0 | 00 |
| shra | 000010 | 000100 | 10 | 0111 | 01 | 0 | 1 | 0 | 0 | 00 |
| shrav | 000010 | 000101 | 10 | 0111 | 00 | 0 | 1 | 0 | 0 | 00 |
| diff | 000010 | 000110 | 10 | 1000 | 00 | 0 | 1 | 0 | 0 | 00 |
| addi | 010000 |  | 10 | 0001 | 10 | 0 | 1 | 0 | 0 | 00 |
| compi | 010001 |  | 10 | 0010 | 10 | 0 | 1 | 0 | 0 | 00 |
| lw | 010010 |  | 01 | 0001 | 10 | 0 | 1 | 1 | 0 | 00 |
| sw | 010011 |  | xx | 0001 | 10 | 0 | 0 | 0 | 1 | 00 |
| b | 100000 |  | xx | xxxx | 10 | x | 0 | 0 | 0 | 10 |
| br | 100001 |  | xx | xxxx | 01 | x | 0 | 0 | 0 | 01 |
| bltz | 100010 |  | xx | 0000 | xx | x | 0 | 0 | 0 | - |
| bz | 100011 |  | xx | 0000 | xx | x | 0 | 0 | 0 | - |
| bnz | 100100 |  | xx | 0000 | xx | x | 0 | 0 | 0 | - |
| bl | 100101 |  | 00 | xxxx | xx | 1 | 1 | 0 | 0 | 10 |
| bcy | 100110 |  | xx | 0000 | xx | x | 0 | 0 | 0 | - |
| bncy | 100111 |  | xx | 0000 | xx | x | 0 | 0 | 0 | - |

TRUTH TABLE FOR BRANCH CONTROL:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Op | Op-code | Zero | Sign | Carry | PCSrc |
| bltz | 100010 | x | 1 | x | 10 |
| bz | 100011 | 1 | x | x | 10 |
| bnz | 100100 | 0 | x | x | 10 |
| bcy | 100110 | x | x | 1 | 10 |
| bncy | 100111 | x | x | 0 | 10 |

For any other combination, PCSrc will be 00.